Oxygen SDR—Data Sheet

Features

- Tunable range: 70 MHz to 6 GHz
- Xilinx Ultrascale+ MPSOC FPGA
- Analog Devices AD9361 RFIC
- 2 USB-C interfaces (1 Upstream Facing Port, 1 Dual Role Port) supporting USB 3.0 speeds
- 2 Phase coherent RX channels
- 2 Phase coherent TX channels
- Expansion socket for optional RF daughtercards (LNAs, mixers, etc.)
- Internal GPS receiver (requires external 3.3V active antenna)
- 12 External 1.8V GPIOs available with a standard pluggable connector

General Description

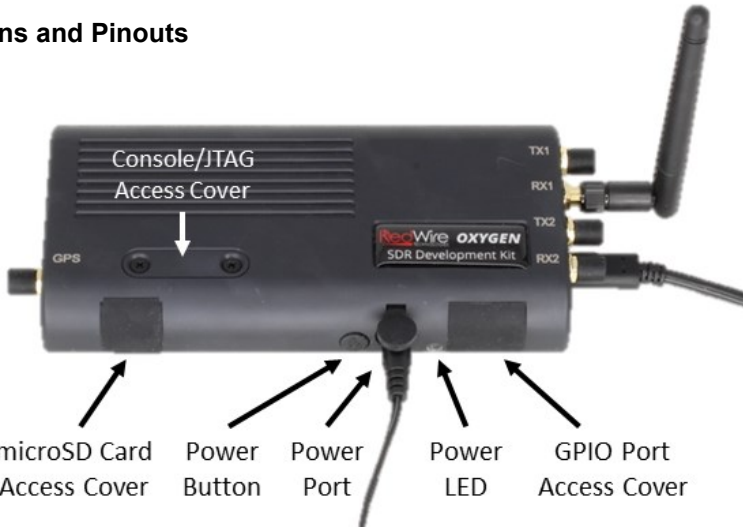
The Oxygen SDR (Software Defined Radio) is built upon an ecosystem of components intended to facilitate the rapid deployment of custom SDRs for mission-specific applications. RWT has generated an initial development board set, the RWT Oxygen SDR Development Kit, to demonstrate how these components can be assembled into a fully embedded fieldable SDR.

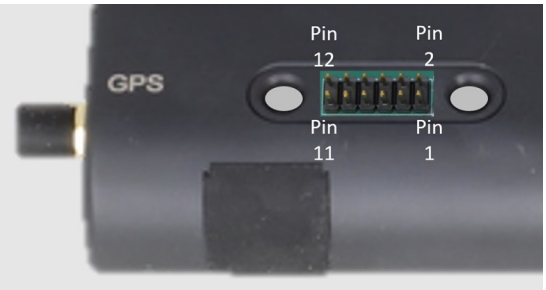
Oxygen SDR can be used to either stream data to a host computer as an iio device over USB gadget ethernet or to operate as a standalone embedded computer. The operating system for the radio is a custom Linux distribution built using the Yocto/OpenEmbedded development system. The development kit includes several options of Xilinx FPGA sizes to allow users to optimize power consumption and performance for their applications. The default RF transceiver card is based on the Analog Devices AD9361 and provides 2TX/2RX MIMO support. Other RF transceiver cards are currently in development and will allow for additional options in the future. The Oxygen SDR includes an integrated GPS receiver, a real time clock, and 12 externally accessible 1.8V GPIO signals.

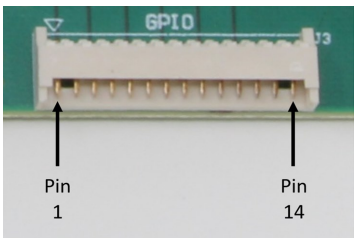
In addition to the radio's standard features, an expansion socket is provided to host application specific RF personality boards if needed. These personality boards are intended to provide additional RF signal processing (e.g., up/down converters, low noise amplifiers, power amplifiers, filters, etc.). Personality boards can be developed by RWT or by customers.

For the latest information including tutorials, examples, and personality board specifications, visit our wiki at:

Connector Locations and Pinouts







Console/JTAG Header Pinout

Header Pin Number	Signal	Direction
1	GND	-
2	GND	-
3	Console UART Tx	Output
4	JTAG TCKn	Input
5	NC	-
6	JTAG V_{cc} Reference	Output
7	Console UART Rx	Input
8	JTAG TDOn	Output
9	NC	-
10	JTAG TDIn	Input
11	NC	-
12	JTAG TMSn	Input

All Console/JTAG header signals use 3.3V logic.

GPIO Header Pinout

Header Pin Number	Signal Name In Linux OS	FPGA Pin
1	GPIO78	B64_L1_P
2	GPIO79	B64_L7_N
3	GPIO80	B64_L3_N
4	GPIO81	B64_L8_P
5	GPIO82	B64_L3_P
6	GPIO83	B64_L8_N
7	GPIO84	B65_L15_N
8	GPIO85	B64_L9_P
9	GPIO86	B65_L15_P
10	GPIO87	B64_L9_N
11	GPIO88	B65_L7_N
12	GPIO89	B64_L4_N
13	1.8V	-
14	GND	-

All GPIO header signals use 1.8V logic.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Input Power Voltage	-0.2 V to 20 V
Input Power Current	< 3A
GPIO Pin Voltage	-0.3 V to 2.1 V
GPIO Pin Current	-12 mA to 12 mA
GPIO Header 1.8V Pin Current	0 mA to 800 mA
RX1 & RX2 Port Input Power (Peak)	< 2.5 dBm
RF Ports DC Voltage (If externally applied)	-50 V to 50 V
GPS Port Active Antenna Current	<50 mA
Operating Temperature Range	-40 C to +70 C

DC Characteristics

Parameter	Min	Typ	Max	Units
Input Power	10	12	15	V
	0.7	1	1.5	A
GPIO Input Low, V_{IL}	0	0	0.45	V
GPIO Input High, V_{IH}	1.27	1.8	1.95	V
GPIO Output Low, V_{OL}	0	0	0.45	V
GPIO Output High, V_{HL}	1.35	1.8	1.95	V
GPS Port DC Bias	3.17	3.3	3.43	V

Sampling Characteristics

Parameter	Min	Typ	Max	Units
RX ADC Resolution		12		bits
ADC Sample Rate			61.44	Msps
TX DAC Resolution		12		bits
DAC Sample Rate			61.44	Msps
TX/RX Channel Bandwidth	0.2		56	MHz

RF Characteristics

Parameter	Min	Typ	Max	Units	Notes
Rx Frequency Range	70		6000	MHz	
Rx Second-Order Input Intercept Point (IIP2)	42	-	85	dBm	Varies with gain and frequency
Rx Third-Order Input Intercept Point (IIP3)	-18	-	16	dBm	Varies with gain and frequency
Rx Noise Figure	2 (800 MHz)	-	5.2 (6 GHz)	dB	Varies with frequency
Rx LO Leakage	-128	-	-92	dBm	Varies with frequency
Rx Phase Error		0.2		degrees	
Tx Frequency Range	46.875		6000	MHz	
TX1 & TX2 RF Output Power	-5	2	9	dBm	
Modulation Accuracy (EVM)		-40		dB	
Tx Third-Order Input Intercept Point (IIP3)	0	-	28	dBm	Varies with gain and frequency
Tx Carrier Leakage		-50		dBc	
Frequency Tolerance	-2	-	+2	ppm	
Frequency Stability	-1	-	+1	ppm	

Physical Characteristics

Parameter	Typ	Units	Notes
Length	180	mm	Including RF connectors
	7.09	in	
	160	mm	Not including RF connectors
	6.31	in	
Width	80	mm	
	3.15	in	
Height	26.33	mm	
	1.04	in	
Weight	462	g	
	1.02	lbs	
Kit Shipping Weight	1.5	kg	Including case and accessories
	3.31	lbs	

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Option	FPGA	ARM A53 Cores	Mali GPU	H.264/5 VCU	Logic Cells	DSP Slices	Block Ram	Ultra RAM
2CG	XCZU2CG-1SFVC784	Dual (1.3GHz)	-	-	103k	240	5.3 Mb	-
3CG	XCZU3CG-1SFVC784	Dual (1.3GHz)	-	-	154k	360	7.6 Mb	-
4CG	XCZU4CG-1SFVC784	Dual (1.3GHz)	-	-	192k	728	4.5 Mb	13.5 Mb
2EG	XCZU2EG-1SFVC784	Quad (1.5GHz)	Y	-	103k	240	5.3 Mb	-
***3EG**	**XCZU3EG-1SFVC784**	**Quad (1.5GHz)**	**Y**	**-**	**154k**	**360**	**7.6 Mb**	**-**
4EV	XCZU4EV-1SFVC784	Quad (1.5GHz)	Y	Y	192k	728	4.5 Mb	13.5 Mb

FPGA Options

Model Designation

OXY: Oxygen SDR

Enclosure Option

MHE: Aluminum Housing

WOE: No Enclosure

FPGA Option

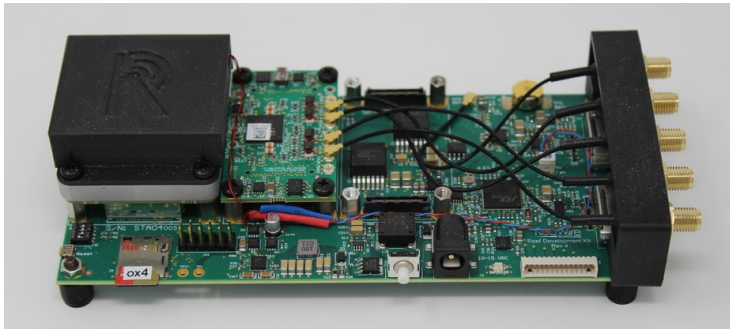
See FPGA Options table

RF Transceiver Option

9361: AD9361 RFIC (2TX/2RX)

9364: AD9364 RFIC (1TX/1RX)

*** The standard configuration comes with the 3EG FPGA module.**



OXY-WOE-xxx-xxxx (no enclosure option)

Ordering Information